ABSTRACT

Disclosed is a charge pump based power supply for use with low voltage dynamic random access memory (DRAM) including a charge pump and a non-overlapping clock signal generator. The charge pump comprises two pump cascades coupled in parallel. Each pump cascade includes a plurality of pump stages connected serially between a supply voltage and an output node. Adjacent stages of each cascade are clocked on opposite phases of the system clock signal. The charge pump drives an output node on the rising and falling edge of the system clock signal. A non-overlapping clock signal generator comprises a charge sharing transistor, controlled by an equalization pulse generated by the outputs of a latch, which equalizes the non-overlapping output clock signals through charge sharing during the non-overlap period between phases of the system clock. The non-overlapping clock signal generator further comprises a transmission gate included to ensure equalization of the non-overlap period.